A 12-GHz 1-W GaAs MESFET Amplifier

MASAAKI NAKATANI, YOSHINOBU KADOWAKI, AND TAKASHI ISHII

Abstract—**A practical method using small signal S_{22} is presented for the design of GaAs MESFET power amplifiers. A five-stage MIC amplifier, which delivers 1-W power output with 27-dB linear gain in the 12-GHz band, was constructed based on this method. Further improvement in the power performance of the amplifier was investigated using newly developed flip-chip MESFET's resulting in 4-W and 2-W power outputs for a unit and a five-stage amplifier, respectively.**

I. Introduction

With the recent advancement of GaAs MESFET device technology, the power output capability of MESFET's has been increasing steadily. The solid-state MESFET power amplifiers developed up to the present in C- to X-band frequencies have performances good enough to replace TWT amplifiers in communication systems [1]–[3]. In the upper X band and higher frequency range, however, few MESFET's providing output powers over 1 W are commercially available and amplifiers for practical use are in the stage of development keeping pace with advances in the performance of MESFET's. In relation to a SHF TV broadcasting system project in Japan, development of MESFET amplifiers in the 12-GHz band is a matter of special concern, which has made a beginning for this work. For the design of the MESFET amplifiers in this frequency range, FET chips are often used in order to minimize parasitics and obtain superior performances [4], [5]. In this work, however, packaged FET's are used from the standpoints of reliability, reproducibility, and feasibility of design.

In this paper, some discrete subjects are treated in the following sequence. First, a practical method on the design of power FET amplifiers is discussed. Next, the experimental results on a 12-GHz 1-W five-stage amplifier built with commercially available packaged MESFET's in house is presented. Finally, the improvement of the power performance of the amplifier is investigated using newly developed flip-chip power MESFET's.

II. A Design Technique of Power FET Amplifiers

As is usually the case with the simple design procedure of FET amplifiers, input and output S parameters of the FET, S_{11} and S_{22}, can be independently treated because of the small feedback term, S_{12} [6]. Both small-signal and large-signal techniques are used to optimize gain, bandwidth, and output power for the design of power FET amplifiers. Input impedance S_{11} is relatively insensitive to input RF power levels, whereas output impedance S_{22} varies significantly with the power level, and some large-signal techniques [7] are required in optimizing output matching circuits of MIC amplifiers. One of the techniques is to fix metal slugs at suitable locations of the output matching circuit. Another method is to design the circuit using S parameters measured under large-signal operating conditions [8], [9]. And the widely used one is to determine optimum load by "Load-Pull Method" [10]. These techniques are, however, rather complicated compared with the design procedures for small signal amplifiers based on easily measurable small signal S parameters.

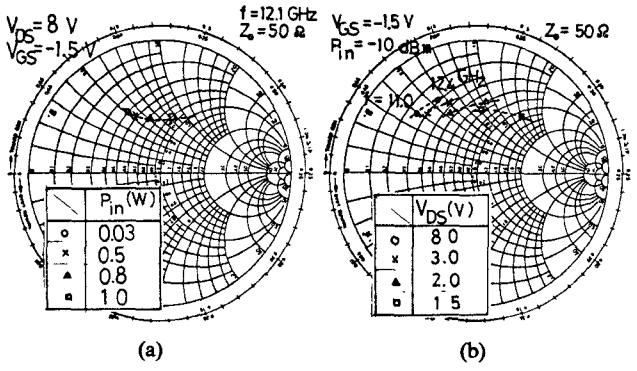


Fig. 1. Dependence of S_{22} on (a) power level, and (b) drain bias.

A. Design Concept

A design concept related to large-signal S parameters was investigated which resulted in the following simple design procedure based on a consideration of an essential operation mechanism of the FET. First, dependence of S_{22} on input RF power levels was examined for a packaged power MESFET of 2400-μm gate width. Fig. 1(a) shows the dependence of S_{22}, measured at 12.1 GHz by means of a standing-wave method, on the power level. The variation of S_{22} could be analyzed [9] as a result of increases in drain conductance g_d and drain-gate feedback capacitance c_{dg} in the well-known small-signal equivalent circuit model of the MESFET; namely, the spreading of the gate depletion layer is considered to become effectively small.

In practical amplifier design procedures, however, it is necessary to measure S_{22} as a function of RF power levels at various frequencies over the bandwidth concerned. A consideration of the behavior of the gate depletion layer leads to a conclusion that the spreading of the depletion layer under large-signal operation is analogous to that under small-signal operation when drain bias is not supplied adequately enough to expand the depletion layer.

Manuscript received April 27, 1979; revised September 24, 1979.

The authors are with the Semiconductor Laboratory, Mitsubishi Electric Corporation, Itami, Hyogo 664, Japan.

0018-9480/79/1200-1066$00.75 ©1979 IEEE

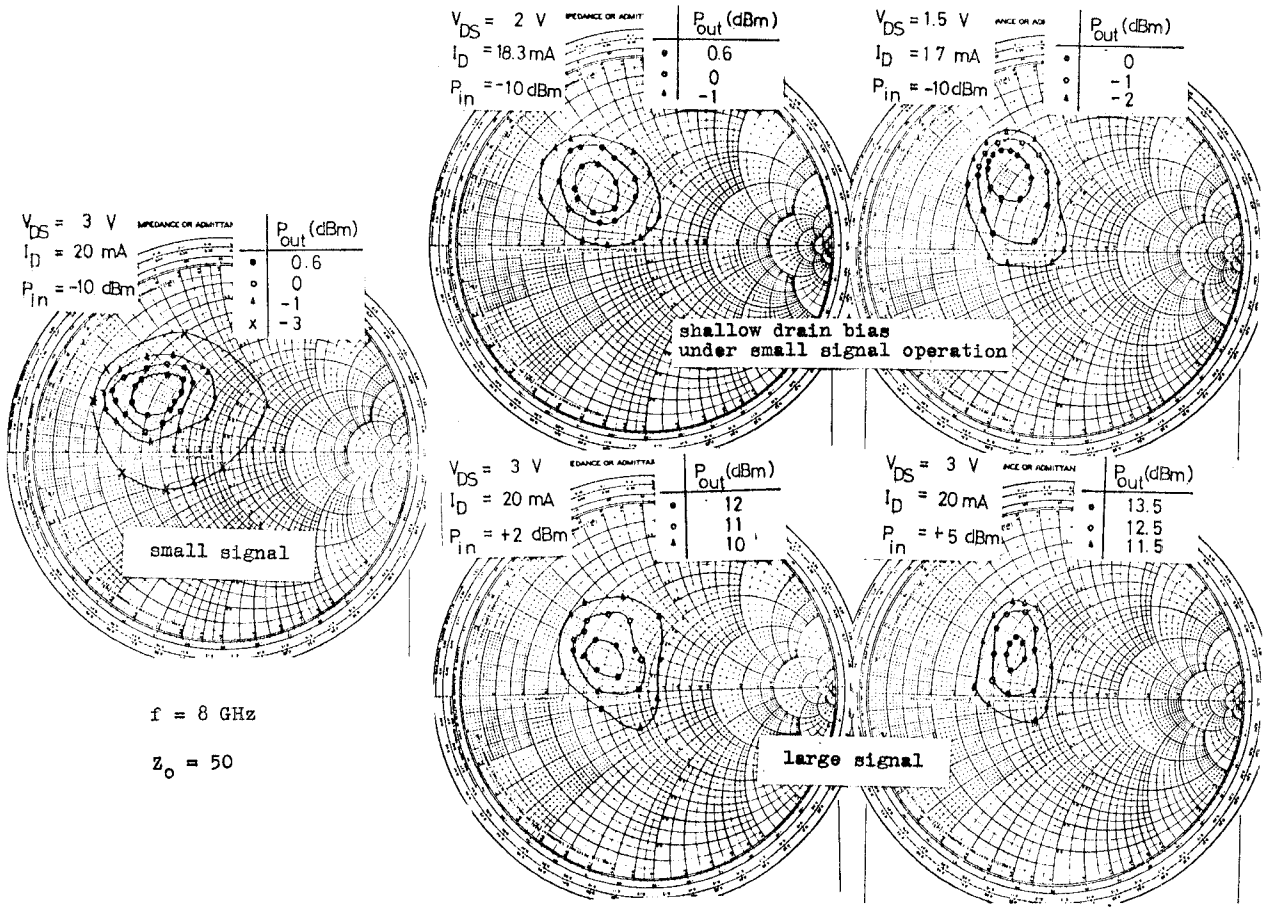


Fig. 2. Load-pulling characteristics of an MESFET depending on input power level and drain bias.

Based on this consideration, the dependence of small signal S_{22} on drain bias conditions at the frequency range of 11.0–12.4 GHz was measured. The result depicted in Fig. 1(b) in contrast to Fig. 1(a) shows that the variation of S_{22} with the increase in RF power levels is similar to that with the decrease in drain bias under small-signal operation. This fact implies that small signal S_{22} measured at a shallow drain bias condition could be used in place of a large signal one in the design of power FET amplifiers.

Furthermore, since FET amplifier performance depends mainly on load impedance, the optimized load impedance should be determined according to whether we aim at maximum power output or maximum small-signal gain. Therefore, load-pulling characteristics were examined in order to find any similarity between the load behavior versus power level and that versus drain bias under small-signal operation. Fig. 2 shows the load pulling characteristics of a MESFET with a total gate width of 400 μm. The measurement of the characteristics was carried out at 8 GHz using a MIC amplifier with a tuner at its output port. The amplifier performance of the FET was the linear gain of 11 dB with the saturation power of 25 mW when operated at the biasing conditions of $V_{DS}=3$ V and $I_D=20$ mA. The input power level was varied over the range from -10 dBm, small-signal level, to $+5$ dBm, large-signal level. On the other hand, the drain bias was varied over the range from 1.5 to 3 V, where the generator impedance of the amplifier is insensitive to the drain bias whereas the S_{22} of the FET varies significantly. The figure implies that the load characteristics behavior versus input power level could also be simulated by varying the drain bias under small-signal conditions. This result means a possibility of realizing an amplifier for maximum output power by designing a small-signal gain matched amplifier using S_{22} under a shallow drain bias condition.

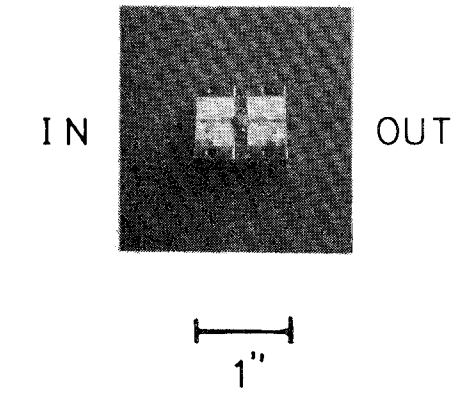


Fig. 3. Photograph of a unit amplifier.

B. Design Example

To ascertain the validity of the design concept described above in practical devices, a single-ended MIC amplifier was built in the 12-GHz band. As is shown in Fig. 3, the amplifier was fabricated on 0.635-mm thick alumina substrates soldered onto a gold-plated brass carrier. First, the operation bias was set with V_{DS} at 8 V and V_{GS} at -1.5 V. Next, the input circuit was gain-

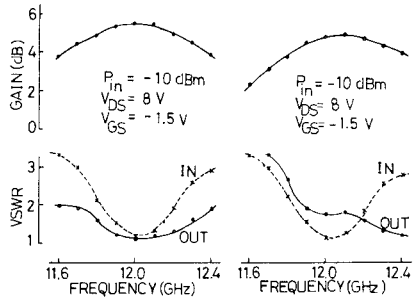


Fig. 4. Small-signal amplifier characteristics of unit amplifiers.

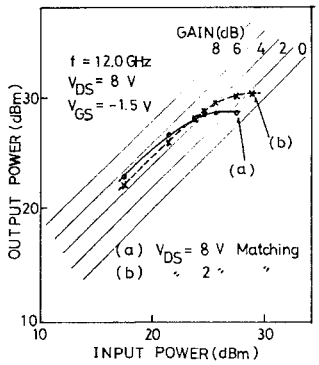


Fig. 5. Power output performances of unit amplifiers.

matched using small signal S_{11}. Finally, a roughly gain-matched output circuit was designed and adjusted by fixing a metal slug at a suitable location of the output matching circuit. The tuning was carried out under small-signal operation at 8 V (case (a)) and 2 V (case (b)) drain biases both with V_{GS} set at -1.5 V. Small-signal amplifier performances for the above mentioned cases are depicted in Fig. 4(a) and (b), respectively. The output-power characteristics of the amplifiers are depicted in Fig. 5. These figures show that case (b) gives lower linear gain and higher power output compared with those for case (a), as is usually the case with the comparison of large-signal to small-signal matching. In fact, the output power in case (b) was found to be nearly equal to the highest one delivered independent of the circuit described above. Thus the validity of the design technique was proved in practical devices. This possible method was utilized throughout this work, leaving more detailed analyses of the technique as a study in the future.

III. A 12-GHz 1-W Amplifier

A. Configuration

The amplifier is composed of five-unit amplifier modules, each of which was built as shown in Fig. 3. An inner view of the amplifier is shown in Fig. 6. As is depicted in the block diagram of Fig. 7, three kinds of MESFET's (Types I, II, and III) were used in this amplifier. Typical electric performances of the MESFET's used are summarized in Table I. The first stage is a balanced module using small-signal Type I MESFET's and 90° interdigitated couplers [11] for low-noise preamplification. The second stage is a single-ended driver composed of a

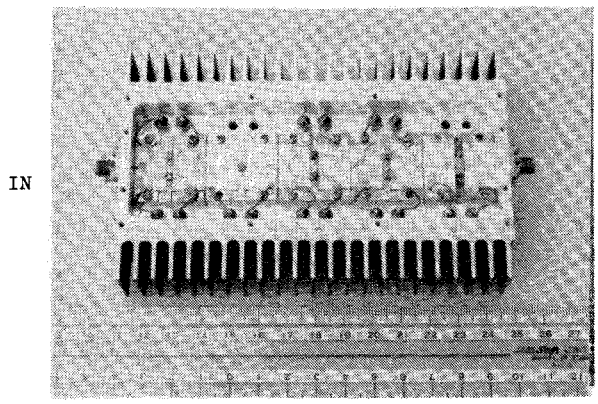
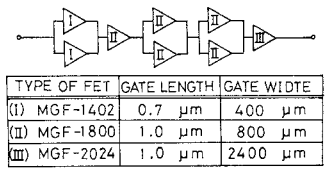


Fig. 6. Photograph of the five-stage MESFET amplifier.



TYPE OF FET	GATE LENGTH	GATE WIDTE
(I) MGF-1402	0.7 μm	400 μm
(II) MGF-1800	1.0 μm	800 μm
(III) MGF-2024	1.0 μm	2400 μm

Fig. 7. Block diagram of the five-stage MESFET amplifier.

TABLE I
Typical Electric Performances of the MESFET's Used in the Five-Stage MESFET Amplifier

TYPE OF FET	I_{DSS}(mA)	g_m(mS)	G_L (dB)	P_{1dB}(mW)
(I) MGF-1402	80	50	9	80
(II) MGF-1800	200	100	8	200
(III) MGF-2024	700	350	4	1000

medium power Type II MESFET. The third and the fourth stages are balanced modules of the Type II MESFET's for medium power amplification. The performances of these medium power amplifier modules are the linear gain of 7.9 dB and 6.0 dB, the power output of 200 mW and 400 mW at 1-dB gain compression and the power added efficiency of 23 and 18 percent for a single-ended module and a balanced module, respectively. The final stage is a single-ended module using a high-power Type III MESFET with air-bridged structure. This high-power module provides the linear gain of 3 dB and the power output of 1.1 W at 1-dB gain compression.

B. Performances

The amplifier was driven with +12-V dc-power supply at 1.2 A and -3 V at 15 mA. The overall characteristics at 12 GHz obtained for the completed five-stage amplifier are the linear gain of 27 dB and the power output of 0.8 W at 1-dB gain compression. The power output of 1 W was obtained with 24-dB gain. Fig. 8 shows the frequency response of the amplifier at various input RF levels. Each curve depicts the gain-bandwidth characteristic corresponding to the linear amplification range, the 1-dB gain compressed condition, and the nearly saturated state. The 1-dB bandwidth at each power level is 500 MHz, 450 MHz, and 350 MHz, respectively. Fig. 9 shows the third-order intermodulation characteristic and AM/PM con-

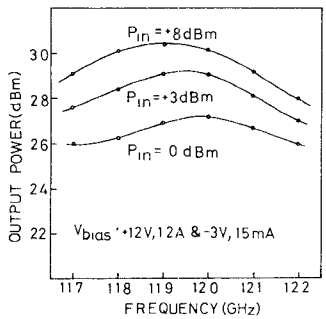


Fig. 8. Frequency response of power gains with input RF power levels as a parameter for the five-stage MESFET amplifier.

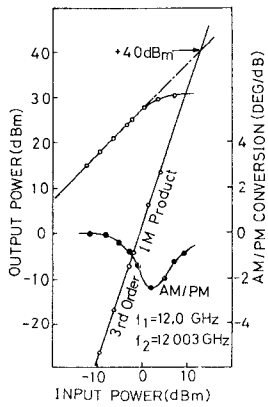


Fig. 9. Third-order intermodulation characteristic and AM/PM conversion at 12 GHz for the five-stage MESFET amplifier.

version performance. The intermodulation characteristic was measured with two equal amplitude carriers 3 MHz apart. The intercept point is +40 dBm. The AM/PM conversion is −2.5°/dB at 1-dB gain compression point. At the frequency of 12 GHz, noise figure was about 6 dB and input/output VSWR's without isolators were less than 2.5:1 for the linear amplification range.

IV. Higher Power Output

A. Flip-Chip Power MESFET

Further improvement of the power performances of the 1-W amplifier described above was investigated using newly developed flip-chip power MESFET's, MGF-2100 series. These MESFET's are fabricated by mounting all electrodes of the FET chip directly on the pedestals of the package. The structure, with no bonding wire leads, minimizes the parasitics, source inductance especially, resulting in an improvement in the gain-bandwidth characteristics as well as power performance and heat dissipation. As a result, such performances as 5.5 W at 10 GHz, 4 W at 13 GHz, and 2.5 W at 15 GHz are obtained for packaged MESFET's [12].

B. Unit Amplifiers

Using some of these flip-chip MESFET's, several unit amplifiers were fabricated for the 12-GHz band frequency. In Table II the linear gain G_L, the output power at 1-dB gain compression point P_{1dB}, the saturation power P_{sat}, and the power added efficiency η_{add} of these

TABLE II
Principal Characteristics of Unit Amplifier Modules Using Flip-Chip Power MESFET's

W_g (μm)	G_L (dB)	P_{1dB} (W)	P_{sat} (W)	η_{add} (%)
2400	5.2	0.93	1.2	18
2400 x 2	4.0	1.95	2.3	14
4800	4.0	2.3	2.6	18
4800 x 2	3.0	3.2	4.0	10

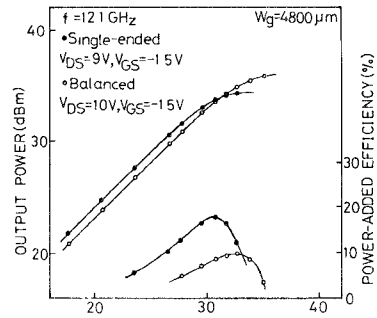
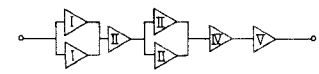


Fig. 10. Power output performances of unit amplifier modules with flip-chip power MESFET's.



TYPE OF FET	GATE LENGTH	GATE WIDTH
(I) MGF-1402	0.7 μm	400 μm
(II) MGF-1800	1.0 μm	800 μm
(IV) MGF-2124	1.0 μm	2400 μm
(V) MGF-2148	1.0 μm	4800 μm

Fig. 11. Block diagram of the five-stage MESFET amplifier improved with flip-chip power MESFET's.

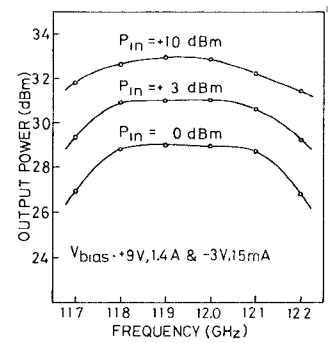


Fig. 12. Frequency response of power gains for the improved five-stage MESFET amplifier.

amplifiers are summarized. For a single-ended 1-W amplifier with a MESFET of 2400-μm gate width, 1-dB bandwidth of 800 MHz, was obtained. Fig. 10 shows, as an example, output power performances for single-ended and balanced amplifiers with MESFET's of 4800-μm gate width. Power output of 4 W was obtained for the balanced type.

C. Five-Stage Amplifier

A five-stage amplifier was constructed using two of these flip-chip MESFET's (Types IV and V). Configuration and performance of this amplifier are shown in Figs.

11 and 12, respectively. Linear gain of 29 dB was obtained with 1.2-W output power at 1-dB gain compression and with 2-W saturation power.

V. Conclusions

A design method for GaAs MESFET power amplifiers has been discussed and a practical method using small signal S_{22} measured at a shallow drain bias condition is presented for the design of output circuits of power FET amplifiers under large-signal operation. Based on this method, a five-stage MIC amplifier with packaged MESFET's was constructed which delivers 1-W power output with 27-dB linear gain and 500-MHz bandwidth in the 12-GHz band. Further improvement of the power performance of the amplifier was investigated using newly developed flip-chip MESFET's. Output power of 4 W is obtained for a balanced unit amplifier and 2 W for a five-stage module.

Acknowledgment

The authors wish to thank Dr. M. Otsubo, A. Nara, T. Suzuki, O. Ishihara, and Y. Mitsui for providing the MESFET's and for helpful suggestions. The authors are also thankful to Drs. S. Mitsui and K. Shirahata for their encouragement of this work.

References

[1] P. T. Ho, "A 7 W C-band FET amplifier using serial power combination techniques," in *1978 IEEE-MTT-S Int. Microwave Symp. Dig.*, pp. 218–220.
[2] W. C. Tsai, "A 5 Watt C-band FET amplifier," in *1978 IEEE-MTT-S Int. Microwave Symp. Dig.*, pp. 285–287.
[3] Y. Saito, S. Akasaka, S. Fukuda, and I. Haga, "6 GHz 5 W GaAs FET power amplifier for 78 Mbits/s 8-phase PSK signal transmission," in *1978 IEEE-MTT-S Int. Microwave Symp. Dig.*, pp. 67–69.
[4] K. B. Nielas, "A 400 mW 11-18 GHz GaAs MESFET amplifier using planar power combining technique," in *IEEE Trans. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 122–123, Feb. 1979.
[5] A. Kayama, M. Matsuzawa, N. Takahashi, I. Haga, S. Aihara, and Y. Fukui, "12 GHz GaAs FET power amplifier for SHF TV signal transmission," Tech. Rep. IECE, vol. 78, no. 226., SSD 78–80, Jan. 1979.
[6] "*S*-parameters circuit analysis and design," Hewlett Packard Application Note 95, 1968.
[7] "Designing MESFET amps for more power," *Microwave System News*, vol. 8, no. 2, pp. 61–66, Feb. 1978.
[8] W. H. Leighton, R. J. Chaffin, and J. G. Webb, "RF amplifier design with large-signal S parameters," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-21, pp. 809–814, Dec. 1973.
[9] Y. Mitsui, M. Nakatani, and S. Mitsui, "Design of GaAs MESFET oscillator using large signal *S* parameters," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-25, pp. 981–984, Dec. 1977.
[10] Y. Takayama, "A new load-pull characterization method for microwave power transistors," in *1976 IEEE-MTT-S Int. Microwave Symp. Dig.*, pp. 218–220.
[11] J. Lange, "Interdigitated stripline quadrature hybrid," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-17, pp. 1150–1151, Dec. 1969.
[12] Y. Mitsui, M. Kobiki, M. Wataze, M. Otsubo, T. Ishii, and S. Mitsui, "A 12 GHz 4 W flip-chip GaAs FET," Tech. Rep. IECE, vol. 78, no. 226, SSD 78–76, Jan. 1979.

Highly Reliable GaAs MESFET's with a Statistic Mean NF_{min} of 0.89 dB and a Standard Deviation of 0.07 dB at 4 GHz

T. SUZUKI, A. NARA, MASAAKI NAKATANI, AND TAKASHI ISHII

***Abstract*—High-performance and high-reliability low-noise GaAs MESFET's are studied from a practical point of view.**

By optimizing the structure and the configuration of GaAs FET's and by developing techniques to form a reproducible thick submicrometer gate, GaAs FET's having improved characteristics have been made.

A mean minimum noise figure NF_{min} of 0.89 dB, a standard deviation of 0.07 dB at 4-GHz CW and a pulse input power capability of more than 0.4 and 2 W, respectively, and a failure rate, supported by field data, of less than 200 FIT have become practical.

Manuscript received April 28, 1979; revised October 10, 1979.

The authors are with the Semiconductor Laboratory, Mitsubishi Electric Corporation, 4-1 Mizuhara, Itami, 664 Hyogo, Japan.

I. Introduction

LOW-NOISE GaAs MESFET's are indispensable for use as microwave amplifiers and oscillators operating in the frequency region over 4 GHz [1]–[3].

Minimum noise figure NF_{min} of 0.6 dB at 4 GHz has been obtained in a laboratory. This value is nearly equal to the value calculated for GaAs FET's with a 0.5-μm gate length [4]. Nevertheless, GaAs FET's with noise figure less than 1 dB at 4 GHz, which are required for low-noise receivers in satellite communication systems, are at present difficult to obtain practically.

0018-9480/79/1200-1070$00.75 ©1979 IEEE